UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,744	08/19/2003	Yoshihiro Nishida	04329.3117	3793

22852 7590 12/19/2005

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,744	NISHIDA, YOSHIHIRO	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07/19/05; 11/23/04 and 08/19/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action responsive to communication filed July 17, 2005. Claims 1-10 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

3. The foreign Japanese prior arts listed on the PTO-1449 (June 19, 2005 and November 23, 2004) have not been considered. There is no apparent nexus between the Abstracts of the cited Japanese prior art and the current claims, it would be improper to indicate consideration of the foreign language documents absent a concise statement of relevance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 are rejected under 35 U.S.C. § 102(b) as being

anticipated by Aucsmith et al. (USPN: 6,243,793); hereinafter Aucsmith.

As per claim 1, Aucsmith teaches the invention as claimed including a computer system comprises a shared memory 106 (e.g. see fig. 3); a first processor 104 which writes writing data into the memory 106 (e.g. see figure 3; column 5, lines 60 et seq.); a second processor is taught as processor 304 (e.g. see figure 2; column 5, lines 61 et seq.), and a controller which instructs the second processor to process the writing data based on attribute data representing an attribute of the writing data is equivalently taught by Aucsmith as the state engine that instructs the second processor 204 how to process information in the memory cell in response to reading the state information recorded in the state recording unit by the first processor (e.g. see column 10, lines 42-52; column 5, lines 62 et seq.; column 6, lines 21 et seq.);

As per claim 2, wherein the attribute data comprises information representing a degree of significance (priority) of the writing data (e.g. see column 9, lines 32 et seq.);

As per claim 3, wherein the controller instructs the second processor to process the writing data when the attribute data represents a degree of significance which is higher that a predetermined degree of significance is equivalently taught as determining if a task with higher priority must be perform, and

instructing the second processor to first perform the higher priority task (e.g. see column 9, lines 32 et seq.);

As per claim 4, wherein the controller comprises an interrupt detector which is incorporated in the second processor and instructs to process the writing data when an interruption is detected (e.g. see column 7, lines 17 et seq.);

As per claim 5, the further limitation of a direct memory controller which performs a transfer of the writing data written by the first processor into the memory to a local memory of the second processor, and notifies the second processor that the transfer is completed after the transfer is taught as Aucsmith to the extent that it is being claimed; for example, Aucsmith discloses remote procedure calls (RPC) to be made between the two computer systems having different processors wherein RPC is the mechanism by which an application on one computer/processor system can use the system services (libraries) on the other. For example, application on the first computer system 150 can use RPC for accessing CPU-intensive routines on the second computer system 350 or vice versa. The RPC interface also allows one computer/processor system to provide system information to the other computer/processor system; noting that Aucsmith also discloses the inter-process communication (IPC) is implemented wherein IPC allows information to be sent between two running tasks on two different computer/processor

systems (e.g. see column 6, lines 55 et seq.);

As per claim 6, Aucsmith discloses determination unit comprises an address determination unit as being equivalent to the memory marking unit for determining whether an address on the memory into which the writing data is written by the first processor is in a predetermined area (e.g. see column 5, lines 3 et seq.);

As per claim 7, see arguments with respect to claim 1; in addition, Aucsmith also discloses a register (state register 500; e.g. see figure 5; column 8, lines 4 et seq.) a write detecting unit which detects that the first processor writes the writing data into the memory and stores in the state register 500 an address on the memory of the writing data, wherein the second processor reads the writing data based on the address stored in the register 500 (e.g. see column 8, lines 18 et seq.);

As per claim 8, Aucsmith discloses a controller as being equivalent to the state engine which instructs the second processor to process the writing data when the address is stored in the register (e.g. see column 8, lines 37 et seq.);

As per claim 9, it encompasses the same scope of invention as to that of claim 1, except that it is drafted as method format rather than apparatus format, the claim is therefore rejected for the same reasons as being set forth above.

As per claim 10, Aucsmith discloses the invention as claimed

including a memory control method for controlling a computer system comprising a memory as being equivalent to shared memory 106 (e.g. see fig. 3); a first processor 104 which writes writing data into the memory 106 (e.g. see figure 3; column 5, lines 60 et seq.); a second processor is taught as processor 304 (e.g. see figure 2; column 5, lines 61 et seq.), and a controller which instructs the second processor to process the writing data based on attribute data representing an attribute of the writing data is equivalently taught by Aucsmith as the state engine that instructs the second processor 204 how to process information in the memory cell in response to reading the state information recorded in the state recording unit by the first processor (e.g. see column 10, lines 42-52; column 5, lines 62 et seq.; column 6, lines 21 et seq.); a register is taught as state register 500; e.g. see figure 5; column 8, lines 4 et seq.), write monitoring means which stores in the register an address on the memory of the writing data, wherein the second processor reads the writing data based on the address stored in the register (e.g. see column 7, lines 17 et seq.; especially lines 59-63, and column 8, lines 34 et seq.).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 4:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/December 07, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100